REMARKS

Claims 1, 3, 4-6, and 8 remain in the application and have been amended hereby. Claims 2, 7, 14, and 15 have been canceled, without prejudice or disclaimer.

Reconsideration is respectfully requested of the objection to Figs. 1 and 2 as not being designated as --Prior Art--.

It is respectfully submitted that Figs. 1 and 2 are designated --(RELATED ART)-- which is submitted to be an equivalent designation.

Reconsideration is respectfully requested of the objection to the Abstract.

It is respectfully submitted that the term "means" in lines 3, 4, 6, and 9 was removed from the Abstract by the Preliminary Amendment mailed June 9, 1999. A copy of that Preliminary Amendment is attached as Exhibit A for the Examiner's convenience.

Reconsideration is respectfully requested of the rejection of claims 1, 4-6, 14, and 15 under 35 USC 102(e), as being anticipated by Peeters, and of the rejection of claims 2, 3, 7, and 8 under 35 USC 103(a), as being unpatentable over Peeters.

Independent claims 1 and 4 have been amended in part

to include the limitations of dependent claims 2 and 7, respectively. Accordingly, the rejection of amended independent claims 1 and 4 will be addressed as a rejection under 35 USC 103(a), as being unpatentable over Peeters.

Features of the address generator of the interleaving unit according to the present invention are a first address data generator for generating first address data (S13 in Fig. 8) at predetermined address intervals (18 addresses for example).

The first address data generator includes a counter (62 in Fig. 8) for counting up to a predetermined number (3 for example) and producing counter outputs (S12 in Fig. 8) and a carry output signal (S14 in Fig. 8), and a multiplier (63 in Fig. 8) for generating the first address data (S13 in Fig. 8) at the predetermined address intervals by multiplying each of the counter outputs (S12 in Fig. 8) by a predetermined value (12 HEX for example).

Further, a second address data generator (65 in Fig. 8) is provided for generating second address data (S15 in Fig. 8) at the predetermined address intervals in synchronism with the carry output signal (S14 in Fig. 8) from the counter (62 in Fig. 8).

Furthermore, an adder (64 in Fig. 8) is provided for generating addresses (WA10 and Fig. 8) at the predetermined address intervals by sequentially adding the second address data

(S15 in Fig. 8) to the first address data (S13 in Fig. 8).

Independent claims 1 and 4 have been amended to recite these features of the present invention.

It is respectfully submitted that Peeters fails to show or suggest the above-noted features of the present invention because, although Peeters inherently teaches some sort of address generation and addition, Peeters is merely disclosing a triangular interleaver formed of a triangular shaped matrix of first-in-first-out memory cells.

Accordingly, it is respectfully submitted that amended independent claims 1 and 4, and the claims depending therefrom, are patentably distinct over Peeters.

The references cited as of interest have been reviewed and are not seen to show or suggest the present invention, as recited in the amended claims.

Favorable reconsideration is earnestly solicited.

Respectfully submitted

COOPER & DUNHAM LLP

Jay H. Maioli
Reg. No. 27,213

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend claims 1,3, 4-6, and 8 by rewriting same to read as follows and cancel claims 2, 7, 14, and 15, without prejudice or disclaimer.

--1. (Twice Amended) An address generator for generating addresses [in a predetermined order] for writing data to a prescribed storage means or reading said data from said prescribed storage means, comprising:

first address data generation means for generating [a plurality of] first address data [having] at predetermined address intervals, wherein said first address data generation means includes a counter for counting up to a predetermined number and producing counter outputs and a carry output signal, and a multiplier for generating said first address data at said predetermined address intervals by multiplying each of said counter outputs by a predetermined value;

second address data generating means for generating second [consecutive] address data [for said first address data every] at said predetermined address [interval] intervals in synchronism with said carry output signal from said counter; and

addition means for generating said addresses [having] at said predetermined address intervals by sequentially adding said second address data to said first address data.

--3. (Twice Amended) The address generator according to Claim [2] 1, wherein said multiplier comprises a shift arithmetic circuit for generating said first address data [having] at said predetermined address intervals by bit shifting predetermined bit positions of [the] said counter outputs of [the] said counter.

--4. (Twice Amended) An interleave unit for rearranging and outputting symbols of a transmit symbol series generated by coding original data comprising:

first address generating means for generating [a plurality of] first address data [having] at predetermined address intervals, wherein said first address data generation means includes a counter for counting up to a predetermined number and producing counter outputs and a carry output signal, and a multiplier for generating said first address data at said predetermined address intervals by multiplying each of said counter outputs by a predetermined value;

second address data generating means for generating second address data [for the first address data every] at said

predetermined address [interval] intervals in synchronism with said carry output signal from said counter; and

addition means for generating addresses [having] at said predetermined address intervals by sequentially adding [the] said second address data to [the] said first address data; and

control means for rearranging and outputting said symbols of said transmit symbol series at random by sequentially assigning said addresses [having] at said predetermined intervals to said transmit symbol series.

--5. (Twice Amended) The interleave unit according to claim 4, wherein said control means comprises:

storage means for storing said transmit series symbol series[,];

writing means for writing said transmit symbol series into said storage means on the basis of said addresses [having] at said predetermined address intervals[,]; and

reading means for reading said transmit symbol series from said storage means in an order different from that of said addresses.

--6. (Twice Amended) The interleave unit according to Claim 4, wherein said control means comprises:

storage means for storing said transmit symbol

series[,];

writing means for writing said symbol series into said storage means in a predetermined write order[,]; and

reading means for reading said transmit symbol series from said storage means on the basis of said addresses [having] at said predetermined intervals.

--8. (Twice Amended) The interleave unit according to Claim [7] 4, wherein

said multiplier comprises a shift arithmetic circuit for generating said first address data [having] at said predetermined address intervals by bit-shifting predetermined bit positions of [the] said counter outputs of said counter.--

7217/58620

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Izumo Hatakeyama

Serial No.: 09/283,188

Filed : April 4, 1999

For : ADDRESS GENERATOR, INTERLEAVE UNIT, DEINTERLEAVE UNIT AND TRANSMISSION UNIT

Group A.U.: 2744

I hereby certify that this paper is being deposited this date with the U.S. Postal Service in first class mail addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Jay H. Maioli June 9, 1999
Jay H. Maioli Date
Reg. No. 27,213

June 9, 1999
1185 Avenue of the Americas
New York, NY 10036
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PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to the initial examination of the above identified application, Applicant respectfully requests that the application be amended as follows.

IN THE SPECIFICATION

Page 7, line 4, change "comprising" to --including--.

Page 9, line 12, change "comprises" to --includes--;

same line, change "generating means" to --generator--;

line14, change "generating means" to --generator--;

line16, change "means for generating addresses" to --address generator--;

line 21, change "generating means" to --generator--;

same line, "generating means" to --generator--;

line 22, change "addition means" to --adder--.

Page 10, line 3, change "comprising" to --including--;

line 4, change "generating means" to --generator--;

line 6, change " generating means" to --generator--;

line 8 change "addition means" to --adder--;

line 16, change "generating means" to --generator--;

same line, change "generating means" to --generator--;

line 17, changes "addition means" to --adder--;

line 22, change "comprising" to --contain--.

Page 11, line 3, change "comprising" to --using--;

line 3-4, change "generating means" to --generator--;

line 5-6, change "generator means" to --generator--;

line 7, change "addition means" to --adder--;

line 15, change "generating means" to --generator--;

line 16, change "generating means" to --generator--;

same line, change "addition means" to --adder--.

Page 21, line 9, change "writs" to --writes--.

Page 48, line 20, change "comprising" to --using--;

line 22, change "deinetrleave" to --deinterleave--.

Page 49, line 8, change "generating means" to --generator--;

same line, change "consisting of" to --using--;

line 10, change "generating means comprising of" to --generator using--;

line 11, change "addition means" to "adder";

line 14, change "generating means" to --generator--;

line 14-15, change "counter means" to --counter--;

line 15 change "addition means" to --adder--;

line 18, change "storage means" to --memory--;

line 22, change "storage means" to --memory--;

line 23, change "generation means" to --generator--.

Page 60, line 16, change "modulation means" to --modulator--

.

Page 61, line 4, change "control means" to --controller--;

line 4-5, change "preservation means" to --storage space--;

line 6, change "storage means" to --memory --.

IN THE ABSTRACT OF THE DISCLOSURE

Line 1, change "a" to --an--;

line 3, change "storage means, comprising" to --memory, using--;

line 4, change "generating means" to --generator--;

line 6, change "generating means" to --generator--;

line 9, change "addition means" to --adder--.

IN THE CLAIMS

Please amend claims 1-14 by rewriting the same to read as follows.

--1. (Amended) An address generator for [, in the case of writing data to a prescribed storage means or reading said data from said storage means,] generating addresses in [an] a predetermined order [predetermined] for writing data to a prescribed storage means or reading said data from said prescribed storage means [said storage means], comprising:

first address data generation means for generating a plurality of first address data having predetermined address intervals;

second address data generating means for generating second consecutive address data for said first address data every said address interval; and

addition means for generating addresses having predetermined intervals [in order] by sequentially adding said second address data to [each of] said first address data.

--2. (Amended) The address generator according to Claim 1, wherein said first address data generating means comprises:

a [first] counter for counting up to a predetermined value and producing a counter output; and

a multiplier for generating a plurality of said first address data having said predetermined address intervals by multiplying each of the counter outputs of said [first] counter by a predetermined value.

--3. (Amended) The address generator according to Claim 2, wherein

said multiplier comprises a shift arithmetic circuit for generating said first address data having said predetermined address intervals by bit shifting predetermined bit positions of the counter outputs of the [first] counter.

--4. (Amended) An interleave unit for rearranging and outputting symbols of a transmit symbol series generated by coding original data[, for each frame at random,] comprising:

first address generating means for generating a plurality of first address data [pieces] having predetermined address intervals;

second address data generating means for generating second [consecutive] address data for the first address data every said address interval; and

addition means for generating addresses having predetermined intervals [in order] by sequentially adding the second address

data to [each of] the first address data; and

control means for rearranging and outputting symbols of said transmit symbol series at random by sequentially assigning addresses having predetermined intervals to said transmit symbol series.

--5. (Amended) The interleave unit according to claim 4, wherein said control means comprises:

storage means for storing said transmit series symbol series, [and writes] writing means for writing said transmit symbol series into said storage means on the basis of addresses having said predetermined intervals, and [reads] reading means for reading said transmit symbol series in an order different from that of said addresses.

--6. (Amended) The interleave unit according to Claim 4, wherein said control means comprises storage means for storing said transmit symbol series, [writes] writing means for writing said symbol series into said storage means in predetermined write order, and [reads] reading means for reading said transmit symbol series on the basis of addresses having said predetermined intervals.

--7. (Amended) The interleave unit according to Claim 4, wherein[:]

said first address data generating means comprises:

a [first] counter for counting up to a predetermined value and producing a counter output; and

a multiplier for generating a plurality of said first address data having said predetermined address intervals by multiplying each of the counter outputs of said [first] counter by a predetermined value.

--8. (Amended) The interleave unit according to Claim 7, wherein[:]

said multiplier comprises a shift arithmetic circuit for generating said first address data having said predetermined address intervals by bit-shifting predetermined bit positions of the counter outputs of said [first] counter.

--9. (Amended) A deinterleave unit for receiving [transmit] transmitted signals [transmitted], in which said transmit signals [is] are obtained by applying [a] predetermined processing to transmit data obtained by rearranging and outputting, for each frame at random, symbols of a transmit symbol series generated by coding original data, and for rearranging symbols of a received symbol series retrieved from said [receive] transmitted signals in [the] an original order, said deinterleave unit comprising:

an address generator [comprising] including:

first data generating means for generating a plurality of first address data having predetermined address intervals;

second address data generating means for generating second consecutive address data for the first address data every said address interval; and

addition means for generating addresses having predetermined intervals [in order] by sequentially adding the second address data to each of the first address data; and

control means for rearranging and outputting symbols of the received symbol series in the original order by sequentially assigning said addresses having predetermined intervals to said received symbol series.

--10. (Amended) The interleave unit according to Claim 9, wherein[:]

said control means comprises storage means for storing said symbol series, [writes] writing means for writing said received symbol series into said storage means on the basis of said address having predetermined intervals, and [reads] reading means for reading said received symbol series in an order different from that of said addresses.

--11. (Amended) The deinterleave unit according to Claim 9, wherein[:]

said control means comprises storage means for storing said received symbols, [writes] writing means for writing said received symbol series into said storage means in the

predetermined write order, and [reads] reading means for reading said received symbol series on the basis of said addresses having predetermined intervals.

--12. (Amended) The deinterleave unit according to Claim 9, wherein:

said first address data generating means comprises:

a [first] counter for counting up to a predetermined value and producing a counter output; and

a multiplier for generating a plurality of said first address data having said predetermined address intervals by multiplying each of the counter [the] outputs of said [first] counter by a predetermined value.

--13. (Amended) The deinterleave unit according to Claim 12, wherein

said multiplier comprises:

a shift arithmetic circuit for generating said first address data having said predetermined address intervals by bit-shifting predetermined bit positions of the [counter] outputs of said [first] counter.

--14. (Amended) A transmission unit for transmitting transmit signals generated be rearranging, for each frame at random, symbols of a transmit symbol series generated by coding

original data, and performing predetermined modulation on the converted data which has been rearranged, said transmission unit comprising:

storage means for storing said transmit symbol series in a predetermined write order for [said] each said frame and reading said transmit symbol series in a read order different from said write order for each of a predetermined number of bits;

preservation means for temporarily preserving converted data of predetermined bits sequentially read in said read order;

modulation means for performing said predetermined modulation on said converted data of predetermined bits [which is] outputted from said preservation means; and

control means for storing said transmit symbol series in the next frame in said storage means while the converted data of the last predetermined bits in the current frame is preserved by said preservation means.--

REMARKS

Claims 1-14 remain in the application with all claims having been amended hereby

Claim 15 remains in the application without amendment.

As will be noted from the Declaration, Applicant is a citizen and resident of Japan and this application originated

there.

Accordingly, the amendments made to the specification are provided to place the application in idiomatic English, and the claims are amended to place them in better condition for examination.

An early and favorable examination on the merits is requested.

Respectfully submitted

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